

**B38DF**

**Lab2**

**Lab Report**

1. **Introduction**

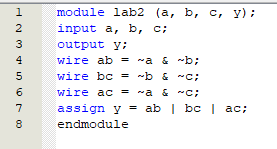
In this lab, students are going to design the combinational and sequential logic circuit using Verilog HDL and give out their waveform simulation results.

1. **Problems**
2. **combinational circuit problem**

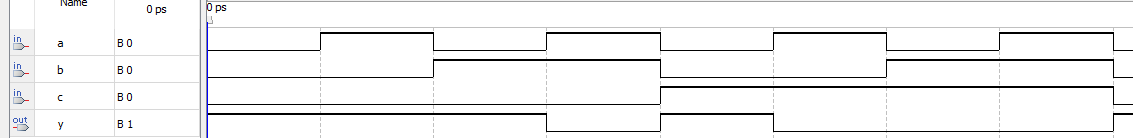
**Solution**

First create the truth table, draw the K-map, simplify it, get y = ~a~b | ~b~c | ~a~c

**Verilog code**



**Simulation result**



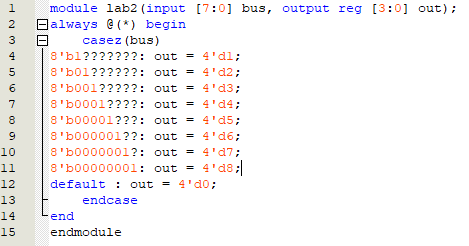
1. **first 1 problem**

**Solution**

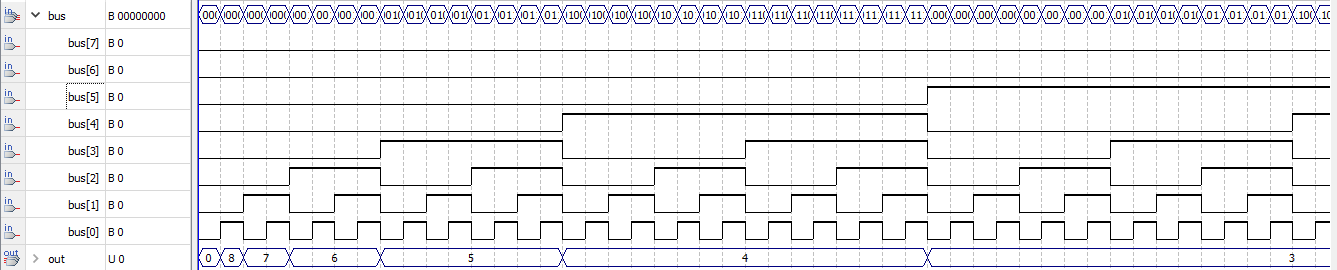
Using the casez according to the hint. It can use “?” to refer to “don’t care”

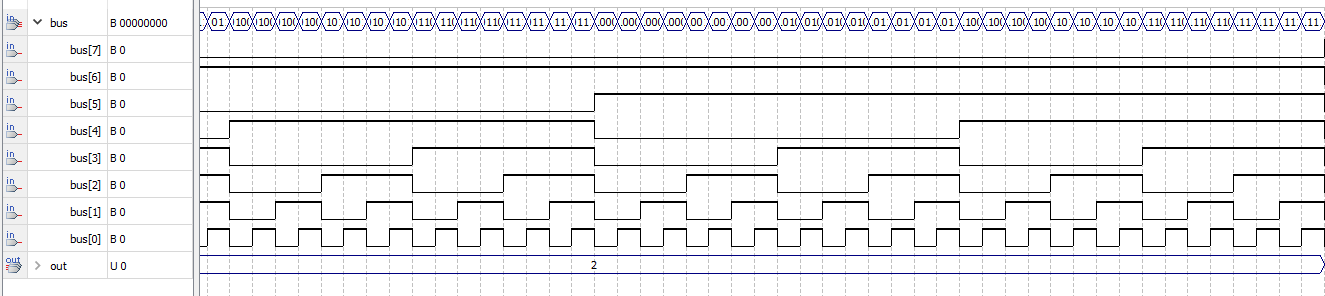
And use 0 to denote there is no 1 in the bus

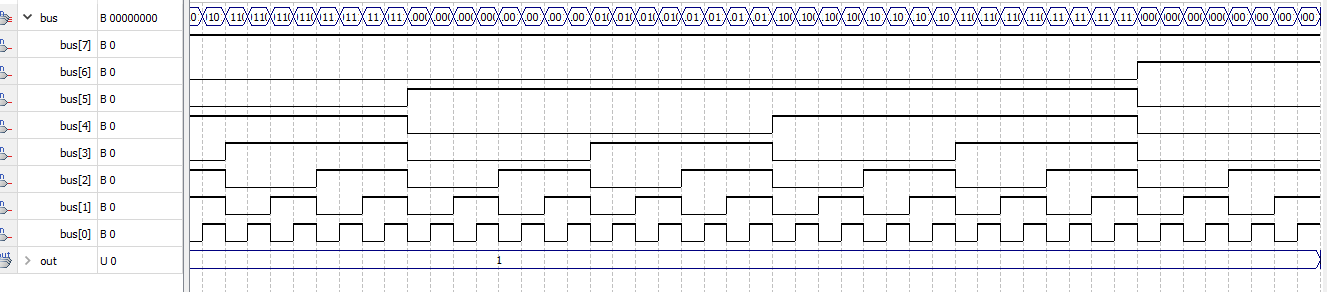
**Verilog code**



**Simulation result**



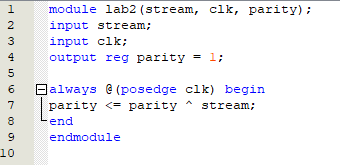




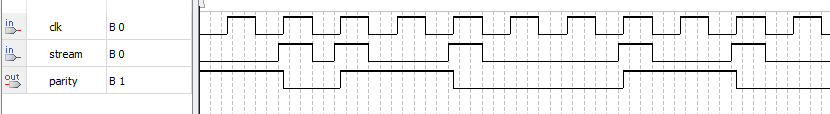
1. **parity check problem**

Use XOR operation to implement the parity check

**Verilog code**

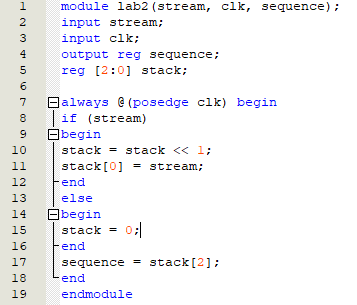


**Simulation result**

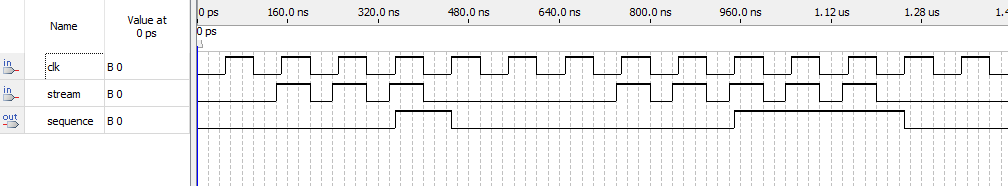


**4)triple 1 problem**

**Verilog code**

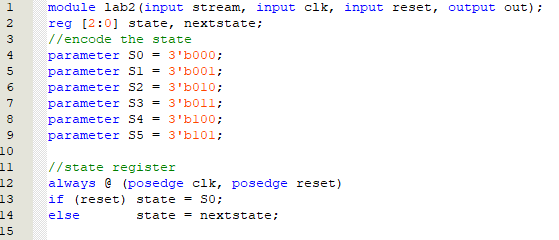


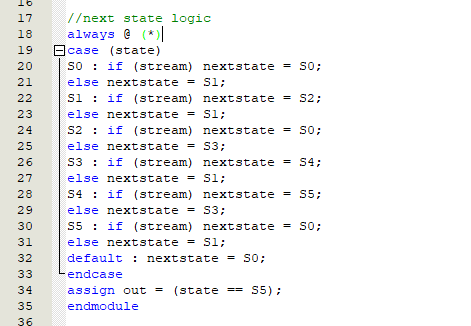
**Simulation result**



**5)number lock problem**

**Verilog code**





**Simulation result**

